

Exercises with Sequential Logic

CS 64: Computer Organization and Design Logic

Lecture #15

Winter 2020

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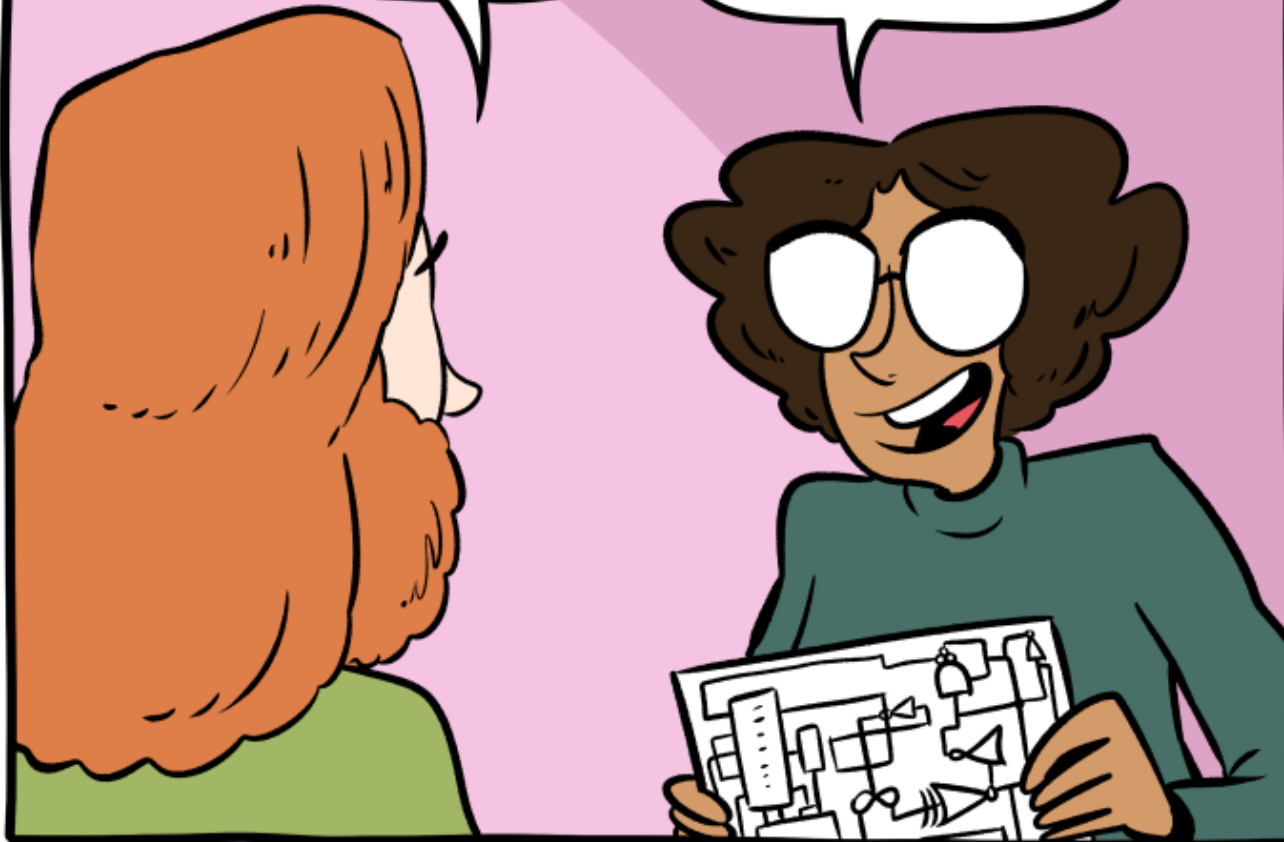
Dept. of Computer Science, UCSB

THIS IS WHAT LEARNING LOGIC GATES FEELS LIKE

SEE, YOU JUST CONNECT THIS 12 INPUT REVERSE FLIP-FLOP TO THE CONTROLLED TWO-THIRDS ADDER, WHICH RESETS THE LATCHES IN THE NOT-NAND RELAY ARRAY, THEN LOOP BACK TO ODD-NUMBER INPUTS AND REVERSE ALL YOUR SWITCHES!

AND WHAT'S THAT DO.?

SUBTRACTION.



Administrative

- Lab 8 will be posted today
- Final Exam Info:
 - **Tuesday, March 17th at 7:30 PM** in this classroom
 - Arrive 10 mins early – randomized seating...
 - Cumulative Exam
 - Study guide/example Qs will be issued by this weekend
 - More details to follow

Lecture Outline

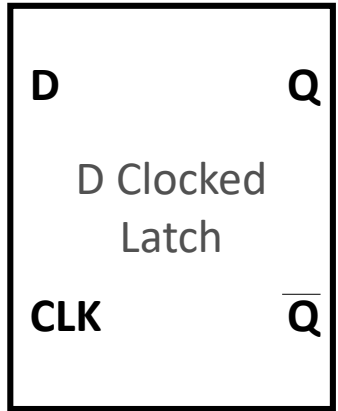
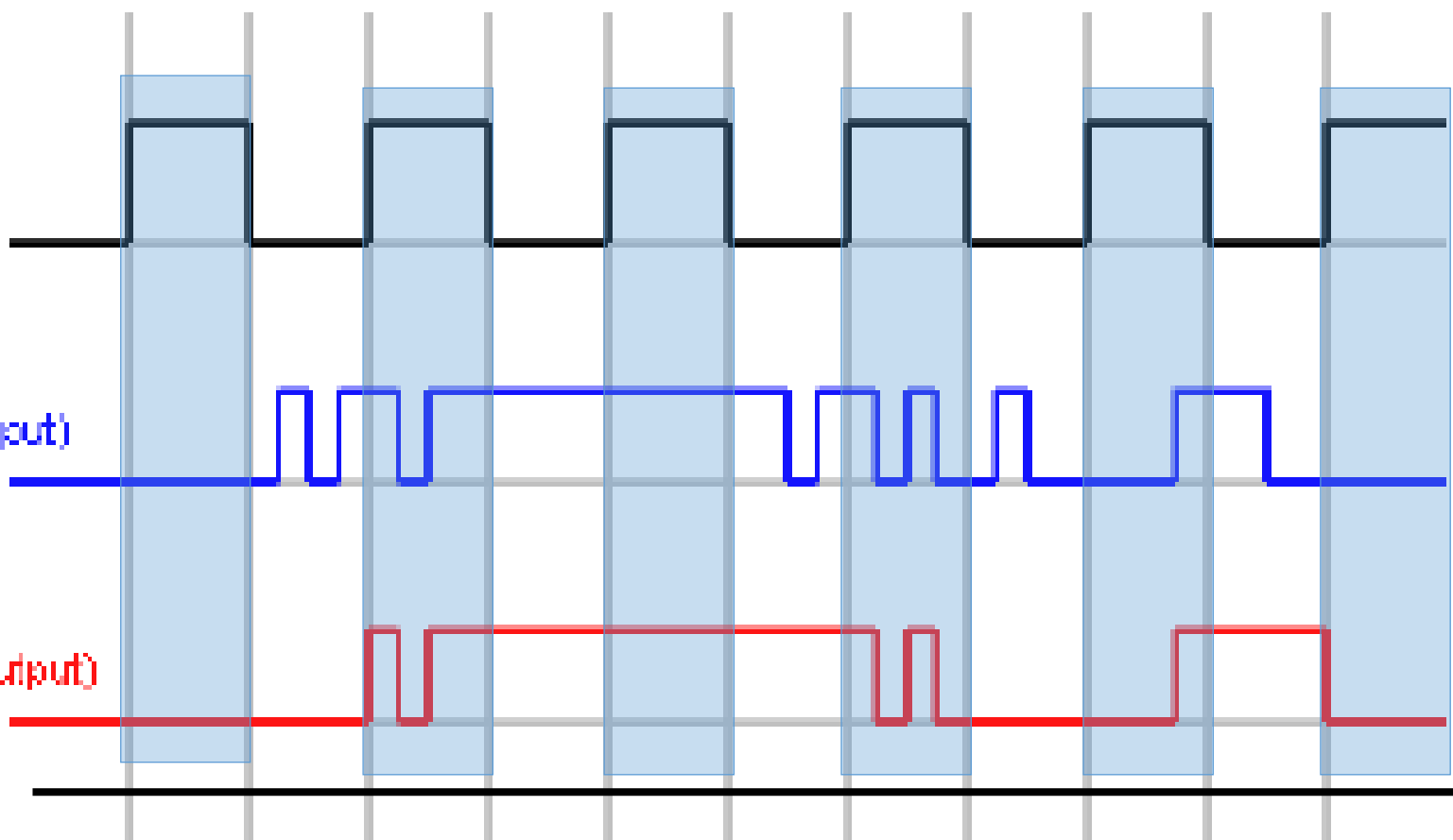
- Exercises with Sequential Logic

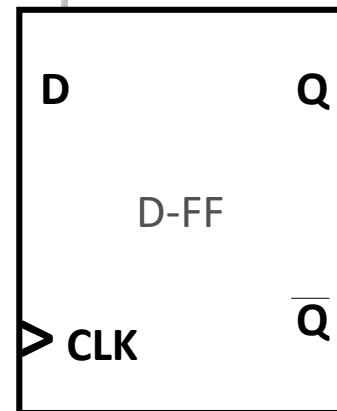
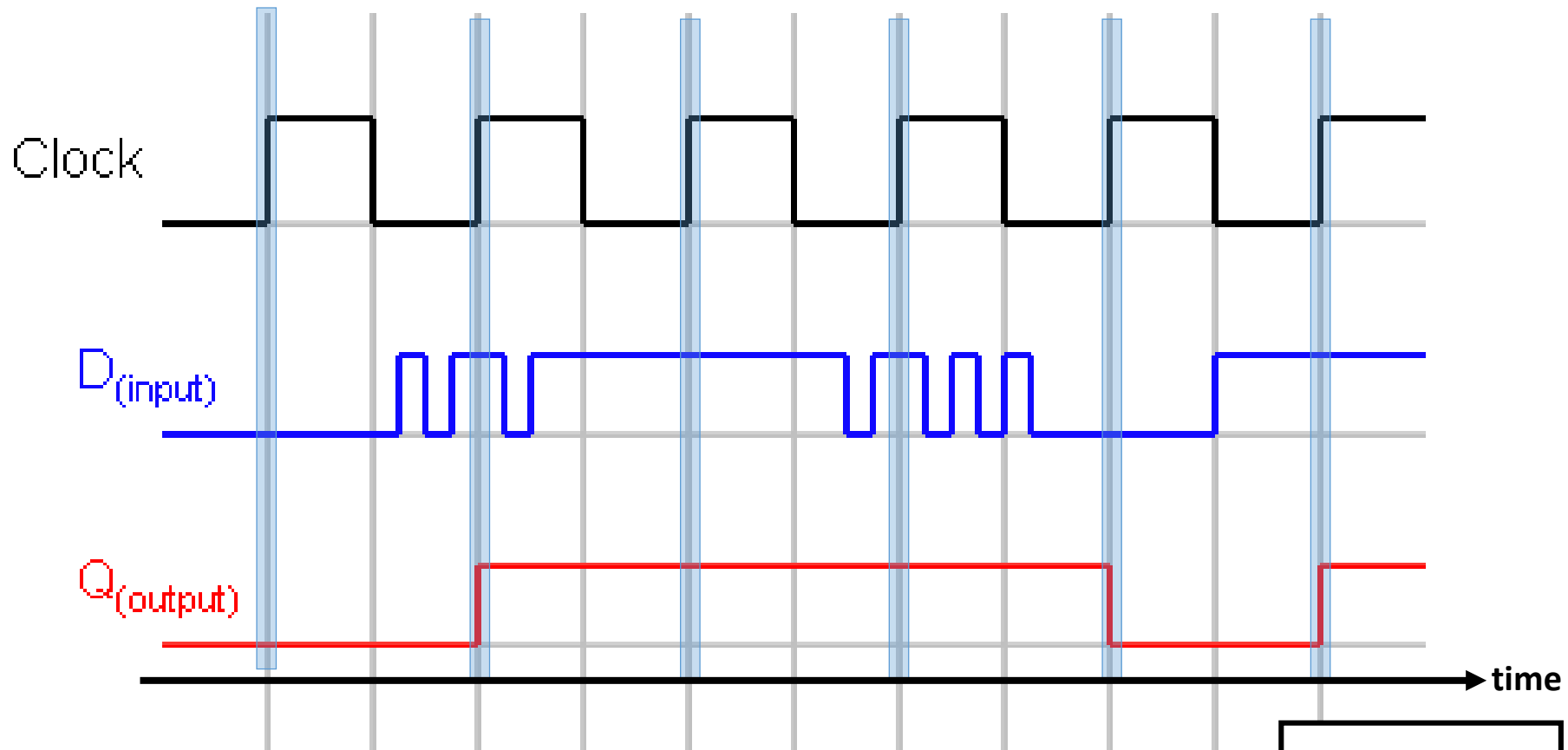
Clock

D (input)

Q (output)

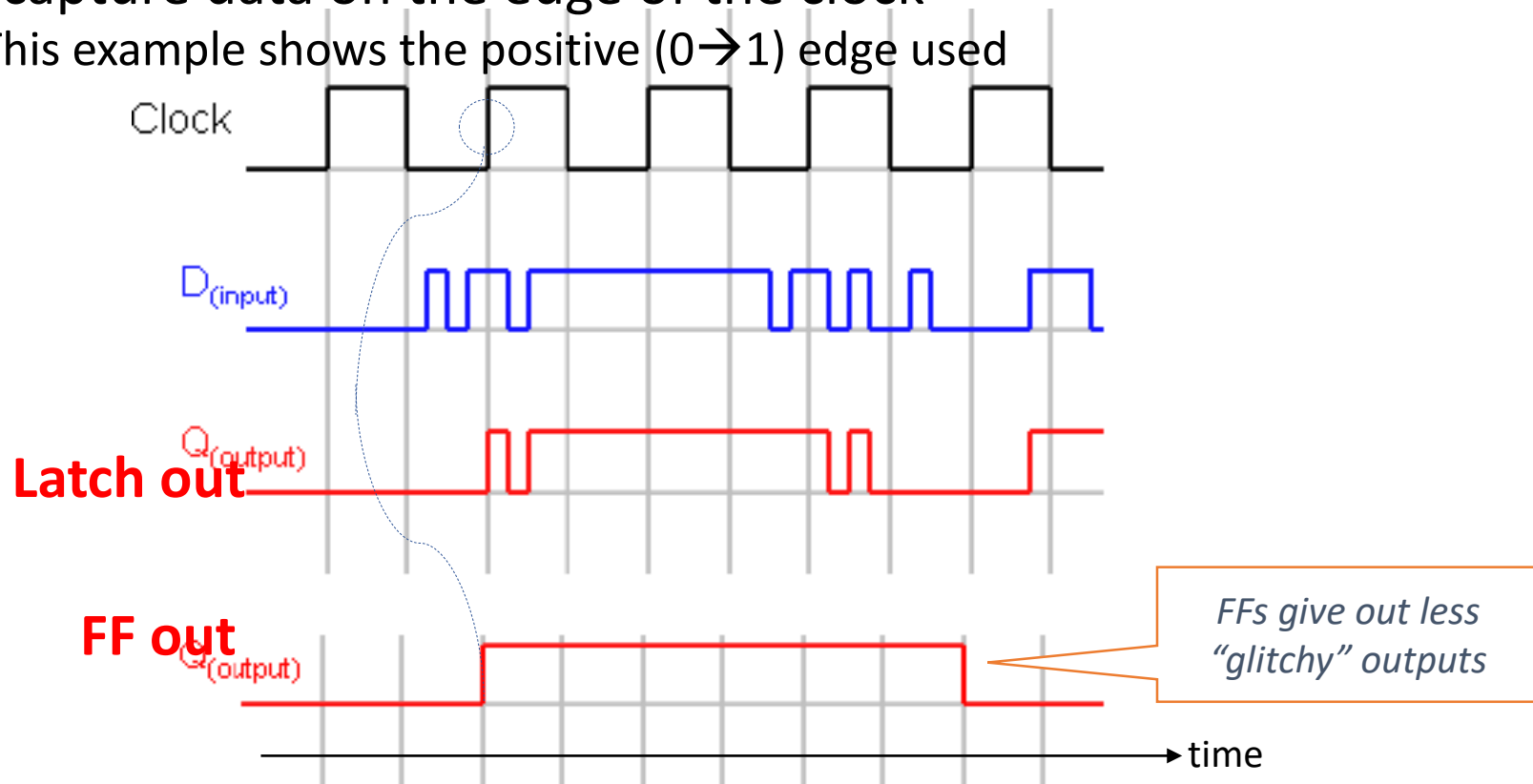
time



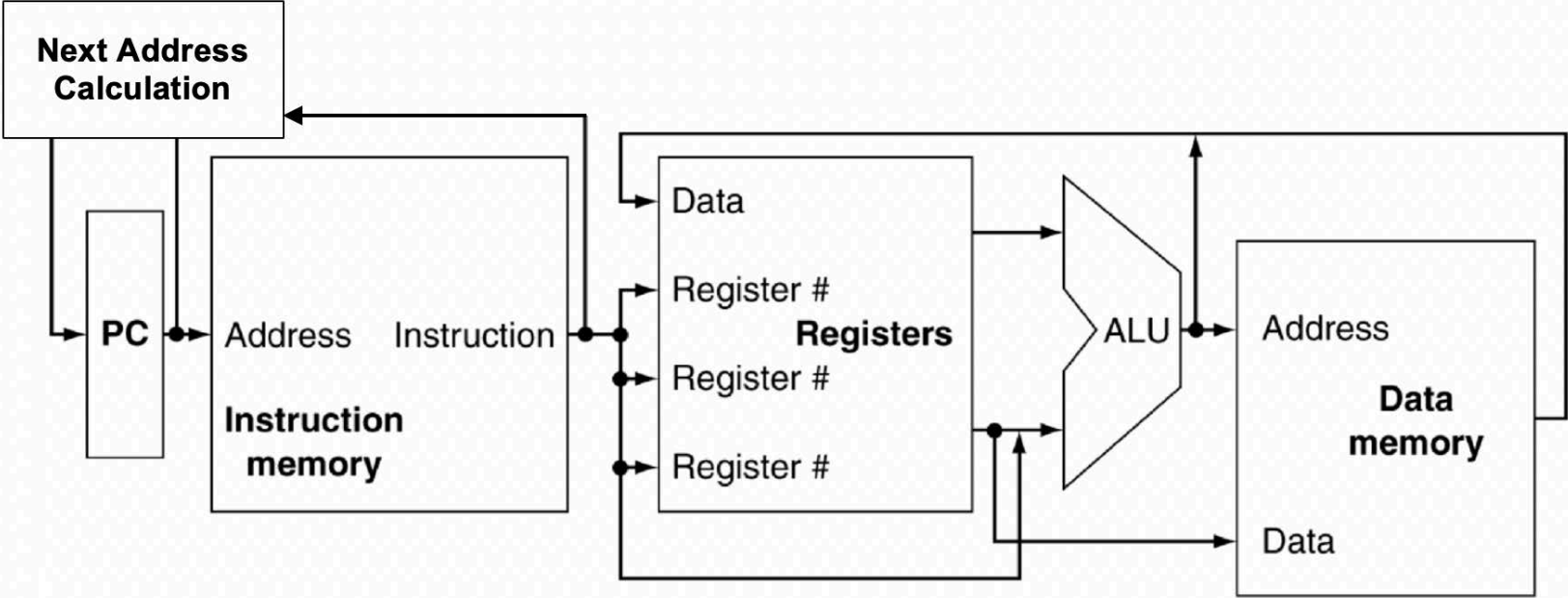


Latches vs. FFs

- Latches capture data on an entire 1 or 0 of the clock
- FFs capture data on the edge of the clock
 - This example shows the positive ($0 \rightarrow 1$) edge used

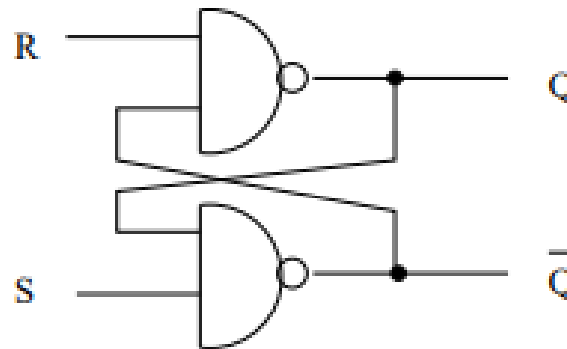


Simplified CPU Block Diagram



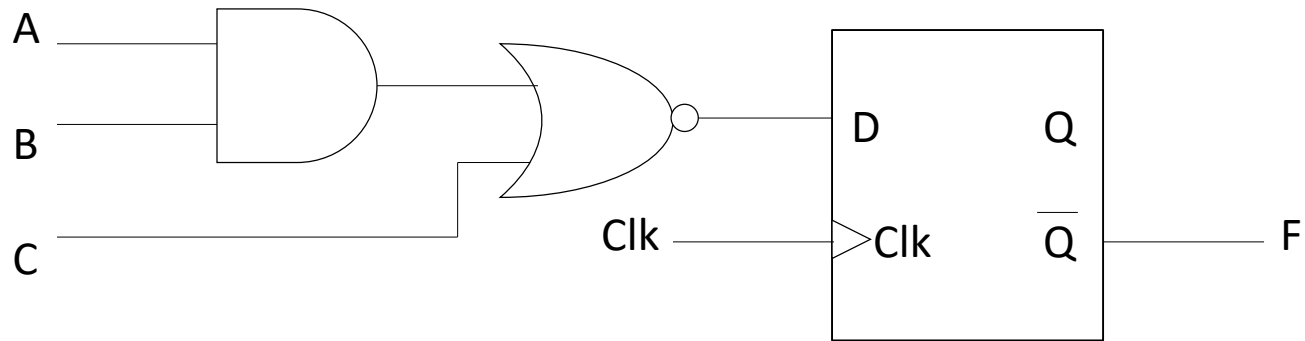
Class Exercise 1

The figure below shows an RS latch made out of NAND gates (rather than NOR gates). How do Q and \bar{Q} depend on the RS inputs? i.e. verify that the circuit can indeed be used as a RS latch.



Exercise 2

Given waveforms for A, B, C, and Clk (see blackboard), determine the output waveform for F

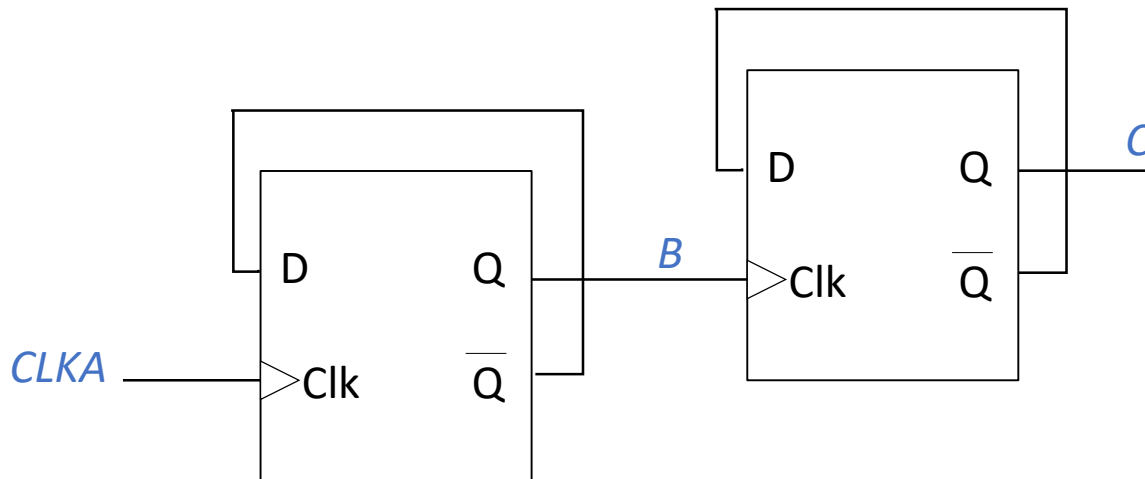


Exercise 3

- Let's design a 3-bit counter using D-FFs and logic gates.
- What's needed:
 - This counts $000 \rightarrow 001 \rightarrow 010 \rightarrow \dots \rightarrow 111 \rightarrow 000$
 - i.e. from 0 to 7 and then loops again to 0, etc...
- Draw the T.T. based on this description
 - How many inputs? How many outputs?
 - Figure out what the “next states” look like based on “current states”
- Draw K-Maps and find optimal output functions

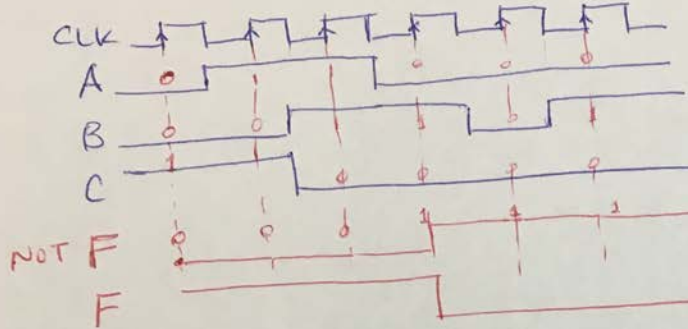
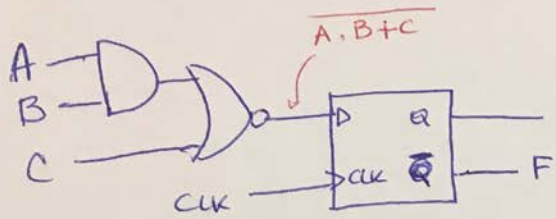
Exercise 4

- Draw the waveforms **B** and **C** for this digital circuit, given CLK_A is a regular clock input.
 - Assume all inputs to the D-FFs are initially at 0.
- What do you conclude about what this does?



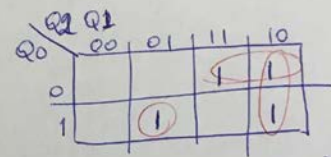
Solutions to Class Exercises 2 and 3 From Lecture 15

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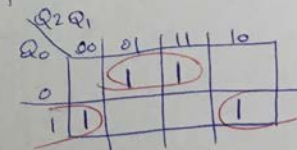
	Current state			Next state		
	Q ₂	Q ₁	Q ₀	Q ₂ [*]	Q ₁ [*]	Q ₀ [*]
0	0	0	0	0	0	1
1	0	0	1	0	1	0
2	0	1	0	0	1	1
3	0	1	1	1	0	0
4	1	0	0	1	0	1
5	1	0	1	1	1	0
6	1	1	0	1	1	1
7	1	1	1	0	0	0

K-Map for Q₂^{*}



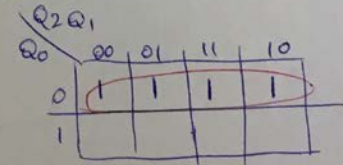
$$Q_2^* = Q_2 \cdot \bar{Q}_0 + Q_2 \cdot \bar{Q}_1 + \bar{Q}_2 \cdot Q_1 \cdot Q_0$$

for Q₁^{*}

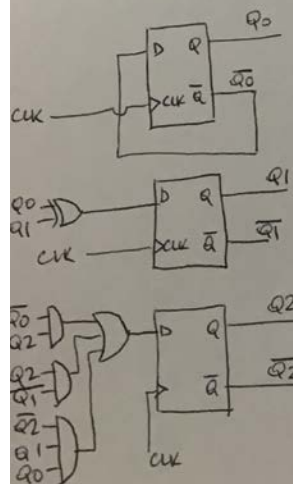


$$Q_1^* = Q_1 \cdot \bar{Q}_0 + \bar{Q}_1 \cdot Q_0 = Q_1 \oplus Q_0$$

for Q₀^{*}



$$Q_0^* = \bar{Q}_0$$



YOUR TO-DOS

- Lab 8

</LECTURE>