Combinatorial Logic

CS 64: Computer Organization and Design Logic
Lecture #13
Winter 2019

Ziad Matni, Ph.D.
Dept. of Computer Science, UCSB

Administrative

- Lab #6
  - Due by ***Monday***

Any Questions From Last Lecture?

Any Questions About the Labs?

5 Minute Pop Quiz!

- Given the following K-Map for binary function **F**:

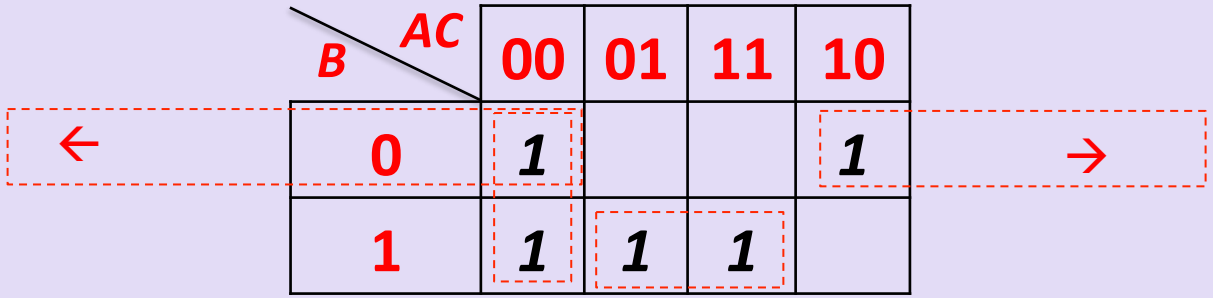
B \ AC	00	01	11	10
0	1			1
1	1	1	1	

a) Group properly and write the optimized function **F**

b) draw the circuit

5 Minute Pop Quiz!

- Given the following K-Map for binary function **F**:



a) Group properly and write the optimized function **F**

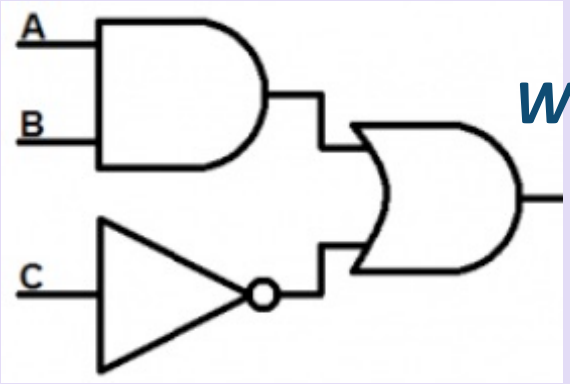
F = !B!C + BC + !A!C

b) draw the circuit

See black board

Combinatorial Logic Designs

- When you *combine* multiple logic blocks together to form a more complex logic function/circuit



What is the output?

$A.B + \overline{C}$

What is its truth table?

A	B	C	F
0	0	0	1
0	0	1	0
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	1

What is its K-Map?

C \ AB	00	01	11	10
0	1	1	1	1
1			1	

Combinatorial Logic

- Combines multiple logic blocks
- The output is a function **only** of the present inputs
- There is no memory of past "states"
  - That is, the output changes *as soon as* any of the inputs change

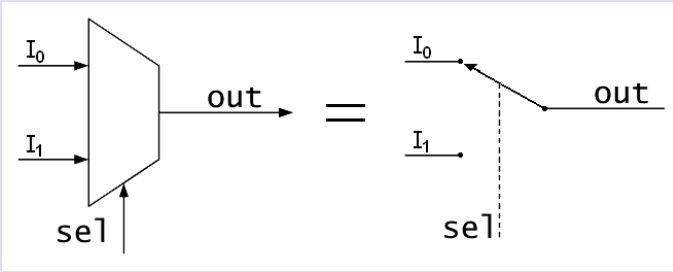
Popular Combinatorial Logic Example: The Multiplexer

- A logical selector:
  - Select either input A or input B to be the output

```
// if s = 0, output is a
// if s = 1, output is b
int mux(int a, int b, int s)
{
   if (!s) return a;
   else return b;
}
```

Multiplexer
(Mux for short)

- Typically has 3 *groups of* inputs and 1 output
  - IN: 2 data , 1 select
  - OUT: 1 data

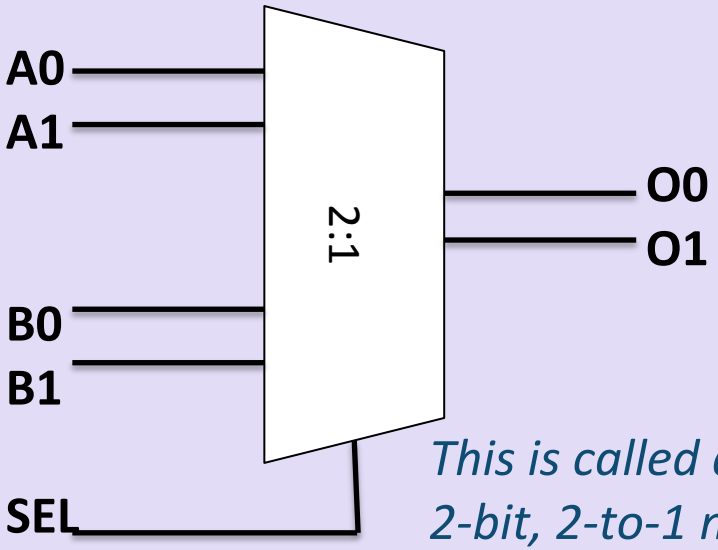


- 1 of the input data lines gets selected to become the output, based on the 3rd (select) input
  - If "Sel" = 0, then I_0 gets to be the output
  - If "Sel" = 1, then I_1 gets to be the output

- The opposite of a Mux is called a **Demulitplexer** (or **Demux**)

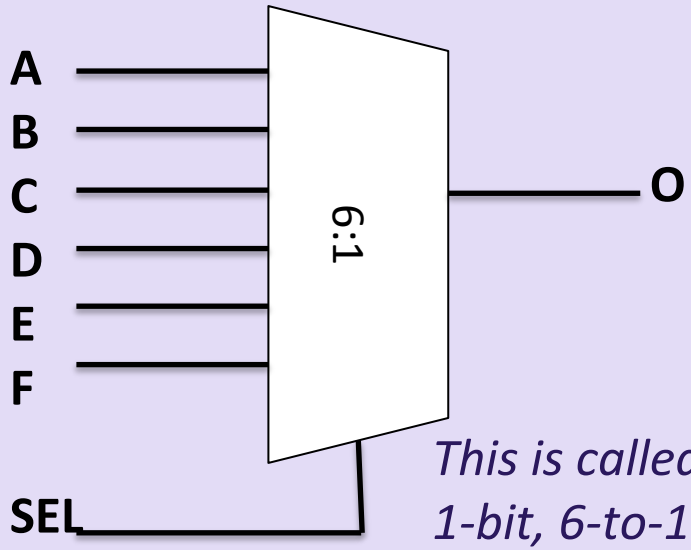
Mux Configurations

Muxes can have I/O that are multiple bits



This is called a 2-bit, 2-to-1 mux

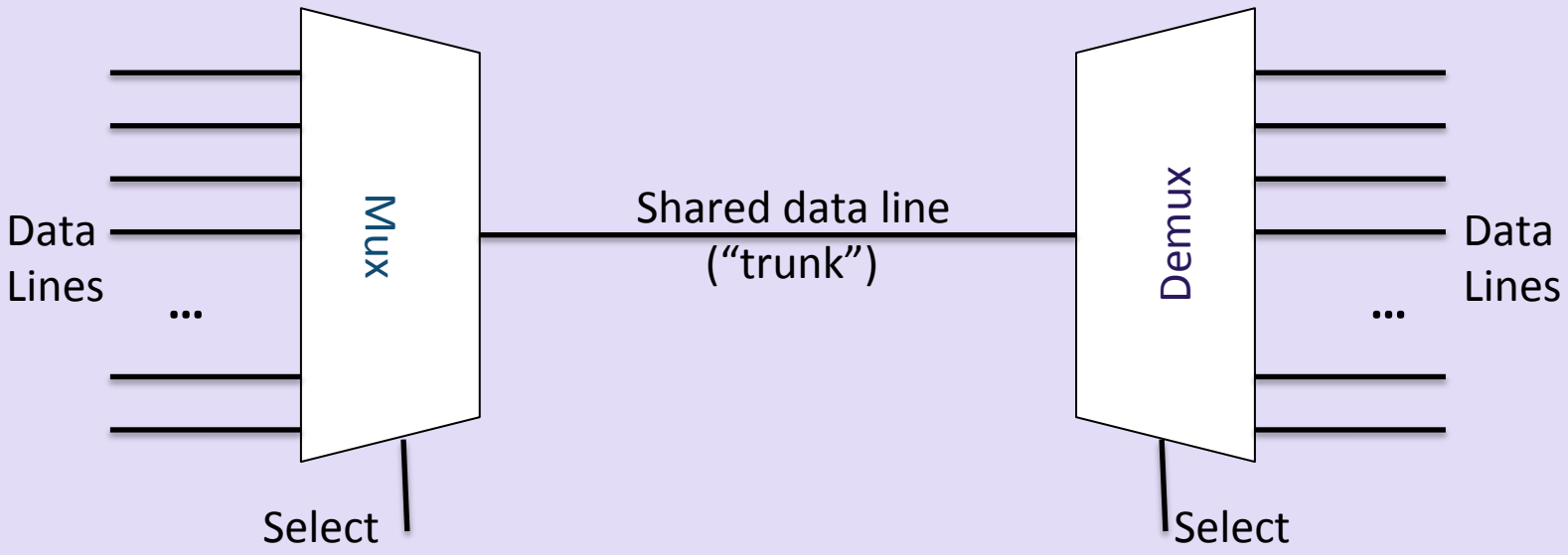
Or they can have more than two data inputs



This is called a 1-bit, 6-to-1 mux

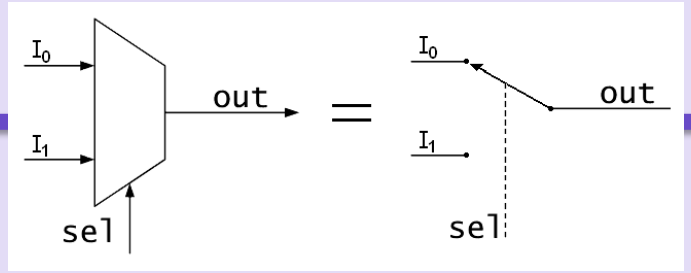
The Use of Multiplexers

- Makes it possible for several signals (variables) to share one resource
  - Very commonly used in data communication lines



Mux Truth Table and Logic Circuit

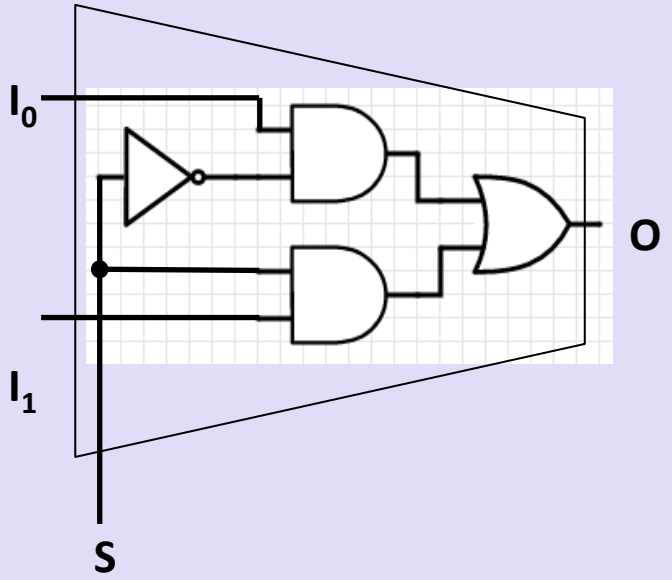
1-bit Mux



I_0	I_1	S	O
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	1

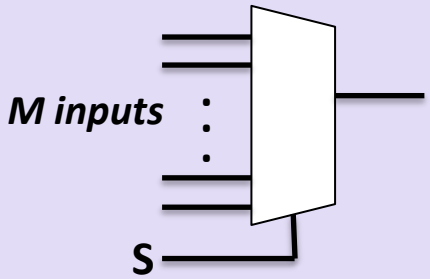
S \ I_0 I_1	00	01	11	10
0			1	1
1		1	1	

$$O = S.I_1 + S'.I_0$$



- = lines are physically connected

Selection Lines in Muxes



- General mux description: **N-bit, M-to-1**
- Where: N = how "wide" the input is (# of input bits, min. 1)
  M = how many inputs to the mux (min. 2)

- The "select" input (S) has to be able to select **1 out of M inputs**
  - So, if M = 2, S should be at least 1 bit *(S = 0 for one line, S = 1 for the other)*
  - But if M = 3, S should be at least **2 bits** *(why?)*
  - If M = 4, S should be ??? *(**ANS**: at least 2 bits)*
  - If M = 5, S should be ??? *(**ANS**: at least 3 bits)*

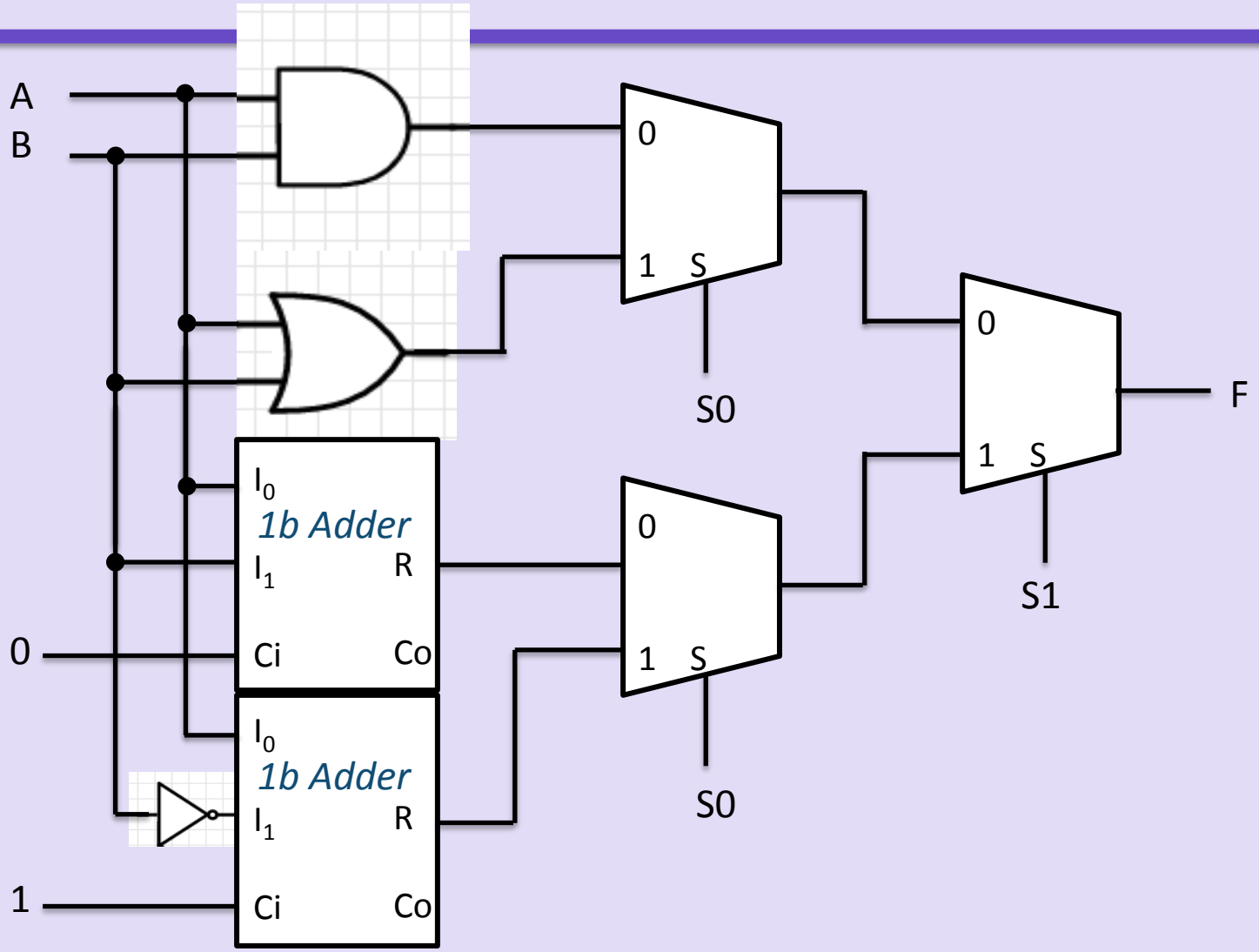
Combining Muxes Together

Can I do a **4:1** mux from 2:1 muxes?

Generally, you can do **2^n:1** muxes from 2:1 muxes.

What Does This Circuit Do?

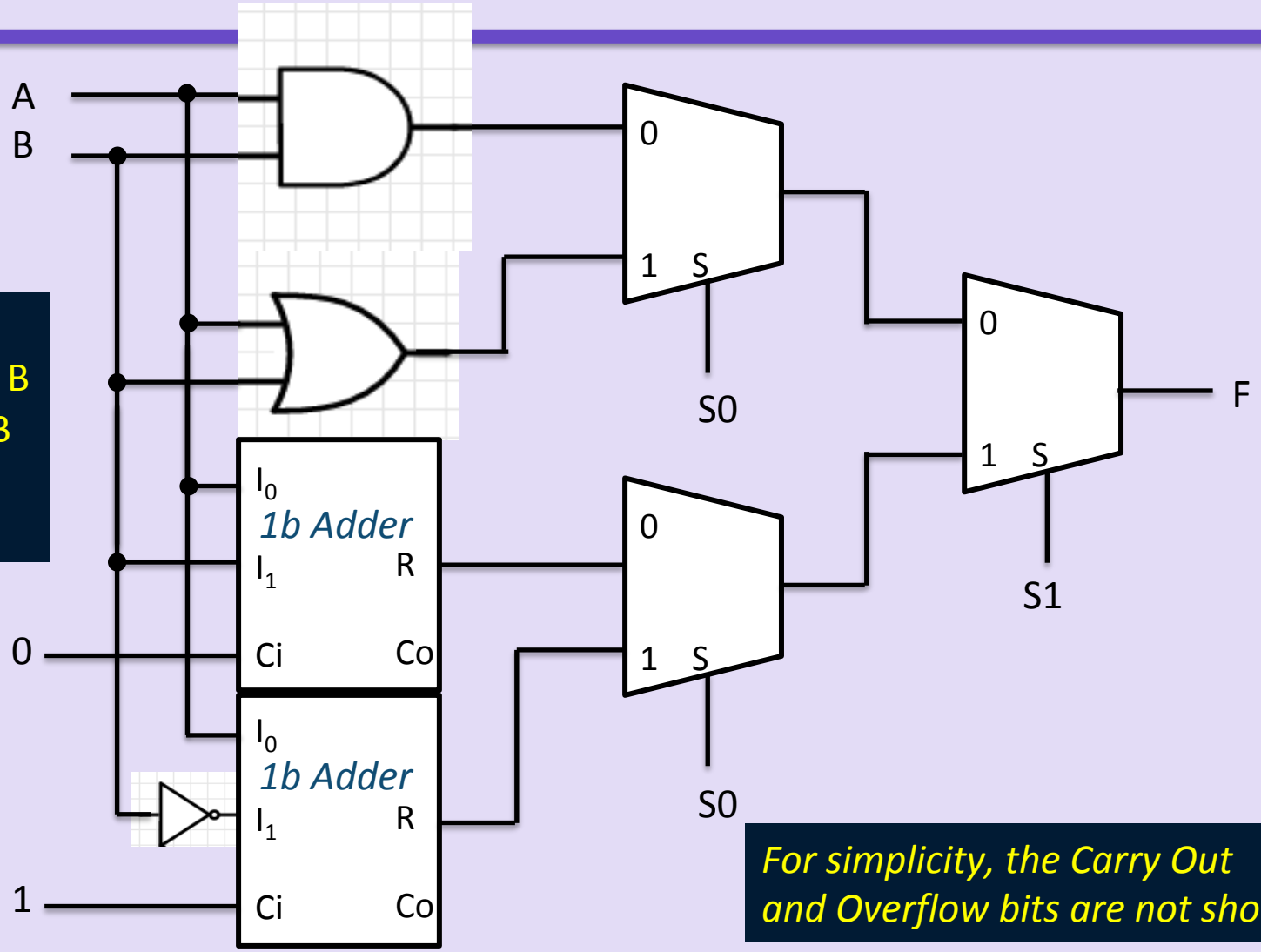
Class Ex.



What Does This Circuit Do?

Class Ex.

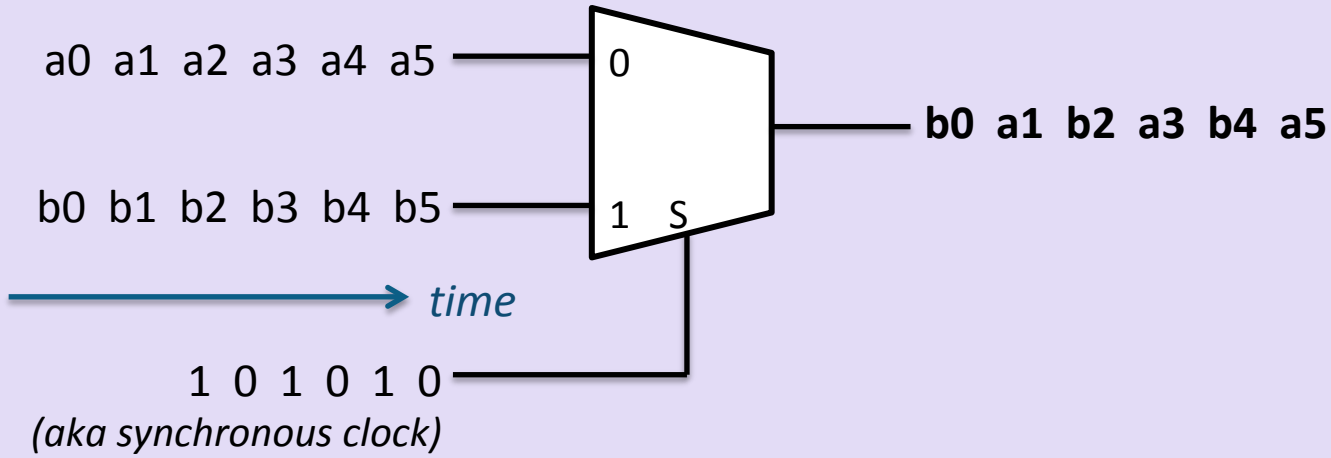
S1	S0	F
0	0	A && B
0	1	A || B
1	0	A + B
1	1	A – B



For simplicity, the Carry Out and Overflow bits are not shown

What Does This Circuit Do?

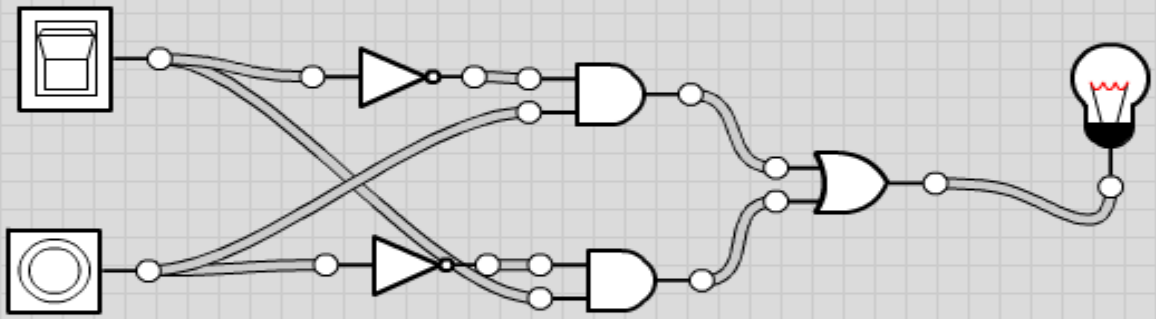
Complete the time-axis diagram…



Input 0	a0	a1	a2	a3	a4	a5
Input 1	b0	b1	b2	b3	b4	b5
Select	1	0	1	0	1	0
Output	b0	a1	b2	a3	b4	a5

time

Simulation of Combinatorial Logic



- Go to:
  https://logic.ly/demo/

IN-CLASS DEMONSTRATION

YOUR TO-DOs

- Lab 6!

</LECTURE>